

Notice of References Cited	Application/Control No. 09/763,204	Applicant(s)/Patent Under Reexamination CLERMIDY ET AL.	
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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
A	A	US-6,646,989 b1	11-2003	Khotimsky et al.	370/238
B	B	US-5,065,308	11-1991	Evans, Richard A.	714/11
C	C	US-6,681,316 B1	01-2004	Clermidy et al.	712/11
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	K	US-			
	L	US-			
	M	US-			

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	S					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
U	U	Chean et al. A Taxonomy of Reconfiguration Techniques for Fault-Tolerant Processor Arrays. IEEE Computer, pages 55-69.
V	V	Roychowdhury et al. Efficient Algorithms for Reconfiguration in VLSI/WSI Arrays. IEEE Transactions, vol. 39, no. 4. pages 480-489.
W	W	Belkhale et al. Reconfiguration Strategies for VLSI Processor Arrays and Trees Using a Modified Diogenes Approach. IEEE Transactions, vol. 41, no. 1. pages 83-96.
X	X	Kung et al. Fault-Tolerant Array Processors Using Single-Track Switches. IEEE Transactions, vol. 38, no. 4. pages 501-514.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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<input checked="" type="checkbox"/>	U	Chen et al. A Comprehensive Reconfiguration Scheme for Fault-Tolerant VLSI/WSI Array Processors. IEEE Transactions, vol. 46, no 12. pages 1363-1371.			
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